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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,627	08/28/2003	Wen Li	M4065.0420/P420-B	5546

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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,627	LI ET AL.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *18-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *18-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08-28-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on August 28, 2003. The information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 26-30 and 31-33 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 26, 27, 31 and 32 contain the limitation "DC signal characteristic" and "DC input waveform" that do not support anywhere in the specification.

4. Claims 28-30 and 33 are depending on the rejected base claim, which is rejected under 35 U.S.C. 112, first paragraph.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 18-25 and 31-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Shinozaki (U.S. Pat. No. 5,990,730).

Regarding claim 31, as best understood, Shinozaki discloses a clock signal received at an output of a delay line (figures 5 and 2), the clock signal comprising: a first signal portion having a periodic signal characteristic, the first signal portion being present during a first power-up time interval when a periodic input waveform is received at an input of the delay line; and a second signal portion having a DC signal characteristic, the second signal portion being present during a second power-down time interval when a DC input waveform is received at the input of the delay line (figures 4 and 5, col. 7, lines 52; col. 8, lines 15+).

Regarding claim 32, Shinozaki disclose the clock signal received at an output of a delay line as defined in claim 31 wherein the periodic waveform and the DC waveform are received from a switching device during the first and second time intervals respectively (figure 5, stop circuit 49 switching on/off the signal to the delay circuit).

Regarding claim 33, Shinozaki disclose the clock signal received at an output of a delay line as defined in claim 31 wherein a power dissipation in the delay line during the first power-up time interval exceeds a power dissipation in the delay line during the second power-down time interval (the second interval (col. 8, lines 18+).

Regarding claim 18, Shinozaki disclose the method of forming a memory integrated circuit comprising: forming a plurality of delay elements on a substrate of a random access memory integrated circuit, each delay element of the plurality including an input and output (forming the delay elements in the lock loop circuit in the substrate of the device); coupling the respective inputs and outputs of the delay elements to one another to form a delay line having a first one and a last one of the plurality of delay elements (coupling the respective inputs and

outputs of the delay elements to one other to form delay line with a predetermine delay time interval); forming a switching device on the substrate (forming the stop circuit); coupling an input of the first delay element to an output of the switching device; forming a clock input terminal of the random access memory integrated circuit on the substrate; coupling a first clock input of the switching device to the clock input terminal (coupling the input clock signal to the input of the stop circuit); forming a mode-control input terminal of the random access memory integrated circuit on the substrate (mode register and start-up period control circuit); and coupling a second control input of the switching device to the mode-control input terminal, the mode-control terminal being input adapted to receive a power-up/power-down signal (coupling the control signal to the stop circuit in conjunction with the mode register to control the operating mode of the device).

Regarding claim 19, Shinozaki disclose the method of forming a memory integrated circuit as defined in claim 18 further comprising; forming an electric power input terminal on the substrate; and coupling each the delay element to the electrical power input terminal, the plurality of delay elements being adapted to draw a first quantity of power through the electric power input terminal during a first time interval and a second quantity of power through the electric power input terminal during a second time interval, the second quantity of power being greater than the first quantity of power, the second time interval corresponding to a power-up state of the power-up/power-down signal (Vcc supplying to the device through the power terminal of the device then supplying to each of the element in the circuit to perform their function).

Regarding claims 20-25, the apparatus as previously discussed in claims 31-33 would perform the method as claimed in claims 20-25. Therefore, they are analyzed as previously discussed with respect to claims 31-33.

7. Claims 26-30 and 34-37 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art (AAPA).

Regarding claim 34, AAPA figure 1 discloses a memory integrated circuit device comprising: memory logic array (memory logic circuit 82); and a delay locked loop circuit (delay lock loop circuit 80), the delay locked circuit including a delay line having an input and an output (delay line having input 72 and output at 70); and controlling means for controlling an externally generated periodic clock signal, the controlling means coupled to the input of the delay line (clock signal receiving from the controller; see the col. 3, lines 30+ of parent patent #6,438,060).

Regarding claim 35, AAPA discloses the memory integrated circuit device as defined in claim 34 wherein the controlling means comprises: a transistor adapted to alternately block and pass the externally generated periodic clock signal (inherently, all of the control circuit is having a transistor to activate or to deactivate (turn on/off) the control signal to the device in the circuit).

Regarding claim 36, AAPA discloses the memory integrated circuit device as defined in claim 34 further comprising: an external clock input adapted to be coupled to a source of an externally generated clock signal, the external clock input being electrically coupled to an input of the controlling means (external clock signal is being input the integrated circuit 40; col. 3, lines 17+ of 6,438,060).

Regarding claim 37, AAPA discloses the memory integrated circuit device as defined in claim 34 wherein the delay line comprises a plurality of delay elements coupled in series with

one another, the plurality of delay elements being adapted to dissipate a first amount of power in response to receiving the periodic clock signal and being adapted to dissipate a second smaller amount of power in response to receiving no clock signal (col. 3, lines 43+ of 6,438,060).

Regarding claims 26-30, the apparatus as previously discussed in claims 34-37 would perform the method as claimed in claims 26-30. Therefore, they are analyzed as previously discussed with respect to claims 26-30.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
March 10, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818